

## In the Specification

Please delete the Paragraph beginning on Page 1, line 5 and replace it with the following Paragraph.

1       - -U.S. Patent Application No. 10/728,627 ~~(TI-34654)~~,  
2   entitled APPARATUS AND METHOD FOR SYNCHRONIZATION OF TRACE  
3   STREAMS FROM MULTIPLE PROCESSORS, invented by Gary L.  
4   Swoboda, filed on even date herewith, and assigned to the  
5   assignee of the present application; U.S. Patent  
6   Application No. 10/729,212 ~~(TI-34655)~~, entitled APPARATUS  
7   AND METHOD FOR SEPARATING DETECTION AND ASSERTION OF A  
8   TRIGGER EVENT, invented by Gary L. Swoboda, filed on even  
9   date herewith, and assigned to the assignee of the present  
10   application; U.S. Patent Application No. 10/729,239 ~~(TI-~~  
11   ~~34656~~), entitled APPARATUS AND METHOD FOR STATE SELECTABLE  
12   TRACE STREAM GENERATION, invented by Gary L. Swoboda, filed  
13   on even date herewith, and assigned to the assignee of the  
14   present application; U.S. Patent Application No. 10/729,650  
15   ~~(TI-34657)~~, entitled APPARATUS AND METHOD FOR SELECTING  
16   PROGRAM HALTS IN AN UNPROTECTED PIPELINE AT NON-  
17   INTERRUPTIBLE POINTS IN CODE EXECUTION, invented by Gary L.  
18   Swoboda and Krishna Allam, filed on even date herewith, and  
19   assigned to the assignee of the present application; U.S.  
20   Patent Application No. 10/729,591 ~~(TI-34658)~~, entitled  
21   APPARATUS AND METHOD FOR REPORTING PROGRAM HALTS IN AN  
22   UNPROTECTED PIPELINE AT NON-INTERRUPTIBLE POINTS IN CODE  
23   EXECUTION, invented by Gary L. Swoboda, filed on even date  
24   herewith, and assigned to the assignee of the present

1 application; U.S. Patent Application No. 10/729,407 (TI-  
2 ~~34659~~), entitled APPARATUS AND METHOD FOR A FLUSH PROCEDURE  
3 IN AN INTERRUPTED TRACE STREAM, invented by Gary L.  
4 Swoboda, filed on even date herewith, and assigned to the  
5 assignee of the present application; U.S. Patent  
6 Application No. 10/729,564 (TI-~~34660~~), entitled APPARATUS  
7 AND METHOD FOR CAPTURING AN EVENT OR COMBINATION OF EVENTS  
8 RESULTING IN A TRIGGER SIGNAL IN A TARGET PROCESSOR,  
9 invented by Gary L. Swoboda, filed on even date herewith,  
10 and assigned to the assignee of the present application;  
11 U.S. Patent Application No. 10/729,400 (TI-~~34661~~), entitled  
12 APPARATUS AND METHOD FOR CAPTURING THE PROGRAM COUNTER  
13 ADDRESS ASSOCIATED WITH A TRIGGER SIGNAL IN A TARGET  
14 PROCESSOR, invented by Gary L. Swoboda, filed on even date  
15 herewith, and assigned to the assignee of the present  
16 application; U.S. Patent Application No. 10/729,639 (TI-  
17 ~~34663~~), entitled APPARATUS AND METHOD FOR TRACE STREAM  
18 IDENTIFICATION OF A PROCESSOR RESET, invented by Gary L.  
19 Swoboda, Bryan Thome and Manisha Agarwala, filed on even  
20 date herewith, and assigned to the assignee of the present  
21 application; U.S. Patent No. 10/729,214 (TI-~~34664~~),  
22 entitled APPARATUS AND METHOD FOR TRACE STREAM  
23 IDENTIFICATION OF A PROCESSOR DEBUG HALT SIGNAL, invented  
24 by Gary L. Swoboda, Bryan Thome, Lewis Nardini and Manisha  
25 Agarwala, filed on even date herewith, and assigned to the  
26 assignee of the present application; U.S. Patent  
27 Application No. 10/729,327 (TI-~~34665~~), entitled APPARATUS  
28 AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PIPELINE  
29 FLATTENER PRIMARY CODE FLUSH FOLLOWING INITIATION OF AN  
30 INTERRUPT SERVICE ROUTINE; invented by Gary L. Swoboda,

1 Bryan Thome and Manisha Agarwala, filed on even date  
2 herewith, and assigned to the assignee of the present  
3 application; U.S. Patent Application No. 10/729,647 (~~TI-~~  
4 ~~34666~~), entitled APPARATUS AND METHOD FOR TRACE STREAM  
5 IDENTIFICATION OF A PIPELINE FLATTENER SECONDARY CODE FLUSH  
6 FOLLOWING A RETURN TO PRIMARY CODE EXECUTION, invented by  
7 Gary L. Swoboda, Bryan Thome and Manisha Agarwala filed on  
8 even date herewith, and assigned to the assignee of the  
9 present application; U.S. Patent Application No. 10/729,401  
10 (~~TI-34667~~), entitled APPARATUS AND METHOD IDENTIFICATION OF  
11 A PRIMARY CODE START SYNC POINT FOLLOWING A RETURN TO  
12 PRIMARY CODE EXECUTION, invented by Gary L. Swoboda, Bryan  
13 Thome and Manisha Agarwala, filed on even date herewith,  
14 and assigned to the assignee of the present application; U.  
15 S. Patent Application No. 10/729,326 (~~TI-34668~~), entitled  
16 APPARATUS AND METHOD FOR IDENTIFICATION OF A NEW SECONDARY  
17 CODE START POINT FOLLOWING A RETURN FROM A SECONDARY CODE  
18 EXECUTION, invented by Gary L. Swoboda, Bryan Thome and  
19 Manisha Agarwala, filed on even date herewith, and assigned  
20 to the assignee of the present application; U.S. Patent  
21 Application No. 10/729,190 (~~TI-34669~~), entitled APPARATUS  
22 AND METHOD FOR TRACE STREAM IDENTIFICATION OF A PAUSE POINT  
23 IN A CODE EXECUTION SEQUENCE, invented by Gary L. Swoboda,  
24 Bryan Thome and Manisha Agarwala, filed on even date  
25 herewith, and assigned to the assignee of the present  
26 application; U.S. Patent Application No. 10/729,196 (~~TI-~~  
27 ~~34670~~), entitled APPARATUS AND METHOD FOR COMPRESSION OF A  
28 TIMING TRACE STREAM, invented by Gary L. Swoboda and Bryan  
29 Thome, filed on even date herewith, and assigned to the  
30 assignee of the present application; U.S. Patent

1 Application No. 10/729,272 ~~(TI-34671)~~, entitled APPARATUS  
2 AND METHOD FOR TRACE STREAM IDENTIFICATION OF MULTIPLE  
3 TARGET PROCESSOR EVENTS, invented by Gary L. Swoboda and  
4 Bryan Thome, filed on even date herewith, and assigned to  
5 the assignee of the present application; and U.S. Patent  
6 Application No. 10/729,191 ~~(TI-34672)~~ entitled APPARATUS  
7 AND METHOD FOR OP CODE EXTENSION IN PACKET GROUPS  
8 TRANSMITTED IN TRACE STREAMS, invented by Gary L. Swoboda  
9 and Bryan Thome, filed on even date herewith, and assigned  
10 to the assignee of the present application are related  
11 applications. - -

12  
13 Please delete the Paragraph beginning on Page 18, line 9 of  
14 the specification and replace that Paragraph with the  
15 following Paragraph.

16  
17 - - The comparator of the present invention is  
18 particularly useful in the test and debug procedures of a  
19 target processor. In analyzing the operation of target  
20 processing system, it is important to know the events that  
21 result in the change in operation produced by a trigger  
22 signal. The present invention captures an identification  
23 of the events that result in the change in operation, e.g.,  
24 the transition to an interrupt service routine. These  
25 events are captured only in the event that an actual  
26 trigger signal is generated. Upon the generation of a  
27 trigger signal, signals specifying the events causing the  
28 trigger signal are stored and can be transferred to the  
29 host processing unit for analysis. In addition, it is

1 necessary to determine where in the program execution the  
2 trigger signal occurred as well as the events that resulted  
3 in the generation of the trigger signal. The contents of  
4 the program counter are the best indication of the state of  
5 program execution at the time of the trigger signal.  
6 However, because of the pipeline delay (and, if present, a  
7 pipeline flattener delay), the events that result in the  
8 generation of the trigger signal are the result of  
9 instructions that began execution before the delay.  
10 Consequently, in order to correlate the events causing the  
11 trigger signal with the appropriate instruction identified  
12 by the program counter, ~~the a~~ delay is added in the  
13 instruction applied to the register. In this manner, the  
14 target processor events resulting in the generation of a  
15 trigger signal and the related position in the instruction  
16 execution can be identified and transferred to the host  
17 processing unit for analysis. In the preferred embodiment  
18 shown in Fig. 2 and Fig. 3, bus A and bus B are both  
19 coupled to the addresses referenced by the program counter.  
20 The comparator unit is then used to generate an EVENT  
21 signal that is applied to the trigger unit. However, the  
22 comparator of the present ~~has~~ invention has wider  
23 application. For example, two addresses can be applied to  
24 the comparator on the two buses and analyzed separately.  
25 ~~For example, a program counter address and an address~~  
26 ~~referenced by the program counter address can be analyzed~~  
27 ~~separately.~~ - -